WHAT IS CLAIMED IS:

1. A method of designing a semiconductor integrated circuit comprising:

a step of connecting one of plural output terminals of a first memory element with a scan data input terminal of a second memory element having a scan test function, on the basis of layout information.

2. A method of designing a semiconductor integrated circuit comprising:

an element connecting step of connecting one of plural output terminals of a first memory element with a scan data input terminal of a second memory element having a scan test function,

wherein said element connecting step includes steps of:

calculating a beeline distance on a substrate from each of said output terminals of said first memory element to said scan data input terminal of said second memory element; and

connecting one of said output terminals of said first memory element having a minimum beeline distance to said scan data input terminal of said second memory element with said scan data input terminal of said second memory element.

3. A method of designing a semiconductor integrated circuit comprising:

an element connecting step of connecting one of plural output terminals of a first memory element with a scan data input terminal of a second memory element having a scan test

function,

wherein said element connecting step includes steps of:

calculating beeline distances on a substrate from said output terminals of said first memory elements to said scan data input terminal of said second memory element;

obtaining a minimum beeline distance among the calculated beeline distances and comparing said minimum beeline distance with another beeline distance;

in the case where a difference between said minimum beeline distance and another beeline distance is equal to or smaller than a predetermined value, calculating fan-out of one of said output terminals of said first memory element having said minimum beeline distance and fan-out of another output terminal of said first memory element having the beeline distance with the difference equal to or smaller than said predetermined value; and

connecting one of said output terminals of said first memory element having minimum fan-out calculated in the previous step with said scan data input terminal of said second memory element.

4. A method of designing a semiconductor integrated circuit comprising:

an element connecting step of connecting one of plural output terminals of a first memory element with a scan data input terminal of a second memory element having a scan test function,

wherein said element connecting step includes steps of:

calculating beeline distances on a substrate from said output terminals of said first memory element to said scan data input terminal of said second memory element;

obtaining a minimum beeline distance among the calculated beeline distances and comparing said minimum beeline distance with another beeline distance;

in the case where a difference between said minimum beeline distance and another beeline distance is equal to or smaller than a predetermined value, load capacitances of one of said output terminals of said first memory element having said minimum beeline distance and another output terminal of said first memory element having the beeline distance with the difference equal to or smaller than said predetermined value; and

connecting one of said output terminals of said first memory element having a minimum load capacitance calculated in the previous step with said scan data input terminal of said second memory element.

5. A method of designing a semiconductor integrated circuit comprising:

an element connecting step of connecting one of plural output terminals of a first memory element with a scan data input terminal of a second memory element having a scan test function,

wherein said element connecting step includes steps of:

calculating wire lengths to be laid from said output terminals of said first memory element to said scan data input

terminal of said second memory element; and

connecting one of said output terminals of said first memory element having a minimum wire length with said scan data input terminal of said second memory element.

6. A method of designing a semiconductor integrated circuit comprising:

an element connecting step of connecting one of plural output terminals of a first memory element with a scan data input terminal of a second memory element having a scan test function,

wherein said element connecting step includes steps of:

calculating wire lengths to be laid from said output terminals of said first memory element to said scan data input terminal of said second memory element;

obtaining a minimum wire length among the calculated wire lengths and comparing said minimum wire length with another wire length;

in the case where a difference between said minimum wire length and another wire length is equal to or smaller than a predetermined value, calculating fan-out of one of said output terminals of said first memory element having said minimum wire length and fan-out of another output terminal of said first memory element having the wire length with the difference equal to or smaller than said predetermined value; and

connecting one of said output terminals of said first memory element having minimum fan-out calculated in the

previous step with said scan data input terminal of said second memory element.

7. A method of designing a semiconductor integrated circuit comprising:

an element connecting step of connecting one of plural output terminals of a first memory element with a scan data input terminal of a second memory element having a scan test function,

wherein said element connecting step includes steps of:

calculating wire lengths to be laid from said output terminals of said first memory element and to scan data input terminal of said second memory element;

obtaining a minimum wire length among the calculated wire lengths and comparing said minimum wire length with another wire length;

in the case where a difference between said minimum wire length and another wire length is equal to or smaller than a predetermined value, calculating load capacitances of one of said output terminals of said first memory element having said minimum wire length and another output terminal of said first memory element having the wire length with the difference equal to or smaller than said predetermined value; and

connecting one of said output terminals of said first memory element having a minimum load capacitance calculated in the previous step with said scan data input terminal of said second memory element.

8. A method of designing a semiconductor integrated

circuit comprising:

an element connecting step of connecting one of plural output terminals of a first memory element with a scan data input terminal of a second memory element having a scan test function,

wherein said element connecting step includes steps of:

calculating fan-out of said output terminals of said first memory element; and

connecting one of said output terminals having minimum fan-out with said scan data input terminal of said second memory element.

9. A method of designing a semiconductor integrated circuit comprising:

an element connecting step of connecting one of plural output terminals of a first memory element with a scan data input terminal of a second memory element having a scan test function,

wherein said element connecting step includes steps of:

calculating fan-out of said output terminals of said first memory element;

obtaining minimum fan-out among the calculated fan-out and comparing said minimum fan-out with another fan-out;

in the case where a difference between said minimum fan-out and another fan-out is equal to or smaller than a predetermined value, calculating beeline distances on a substrate from one of said output terminals of said first memory element having said minimum fan-out and from another

output terminal of said first memory element having the fan-out with the difference equal to or smaller than said predetermined value to said scan data input terminal of said second memory element; and

connecting one of said output terminals of said first memory element having a minimum beeline distance calculated in the previous step with said scan data input terminal of said second memory element.

10. A method of designing a semiconductor integrated circuit comprising:

an element connecting step of connecting one of plural output terminals of a first memory element with a scan data input terminal of a second memory element having a scan test function,

wherein said element connecting step includes steps of:

calculating fan-out of said output terminals of said first memory element;

obtaining minimum fan-out among the calculated fan-out and comparing said minimum fan-out with another fan-out;

in the case where a difference between said minimum fan-out and another fan-out is equal to or smaller than a predetermined value, calculating wire lengths to be laid from one of said output terminals of said first memory element having said minimum fan-out and from another output terminal of said first memory element having the fan-out with the difference equal to or smaller than said predetermined value to said scan data input terminal of said second memory element;

and

connecting one of said output terminals of said first memory element having a minimum wire length calculated in the previous step with said scan data input terminal of said second memory element.

11. A method of designing a semiconductor integrated circuit comprising:

a step of connecting one of plural output terminals of a first memory element with a scan data input terminal of a second memory element having a scan test function, on the basis of timing information.

12. A method of designing a semiconductor integrated circuit comprising:

an element connecting step of connecting one of plural output terminals of a first memory element with a scan data input terminal of a second memory element having a scan test function,

wherein said element connecting step includes steps of:

calculating load capacitances of said output terminals of said first memory element; and

connecting one of said output terminals of said first memory element having a minimum load capacitance with said scan data input terminal of said second memory element.

13. A method of designing a semiconductor integrated circuit comprising:

an element connecting step of connecting one of plural output terminals of a first memory element with a scan data

input terminal of a second memory element having a scan test function,

wherein said element connecting step includes steps of:

calculating load capacitances of said output terminals of said first memory element;

obtaining a minimum load capacitance among the calculated load capacitances and comparing said minimum load capacitance with another load capacitance;

in the case where a difference between said minimum load capacitance and another load capacitance is equal to or smaller than a predetermined value, calculating beeline distances on a substrate from one of said output terminals of said first memory element having said minimum load capacitance and another output terminal of said first memory element having the load capacitance with the difference equal to or smaller than said predetermined value to said scan data input terminal of said second memory element; and

connecting one of said output terminals having a minimum beeline distance calculated in the previous step with said scan data input terminal of said second memory element.

14. A method of designing a semiconductor integrated circuit comprising:

an element connecting step of connecting one of plural output terminals of a first memory element with a scan data input terminal of a second memory element having a scan test function,

wherein said element connecting step includes steps of:

calculating load capacitances of said output terminals of said first memory element;

obtaining a minimum load capacitance among the calculated load capacitances and comparing said minimum load capacitance with another load capacitance;

in the case where a difference between said minimum load capacitance and another load capacitance is equal to or smaller than a predetermined value, calculating wire lengths to be laid from one of said output terminals of said first memory element having said minimum load capacitance and another output terminal of said first memory element having the load capacitance with the difference equal to or smaller than said predetermined value to said scan data input terminal of said second memory element; and

connecting one of siad output terminals of said first memory element having a minimum wire length caliculated in the previous step with said scan data input terminal of said second memory element.

15. A method of designing a semiconductor integrated circuit comprising:

an element connecting step of connecting one of plural output terminals of a first memory element with a scan data input terminal of a second memory element having a scan test function,

wherein said element connecting step includes a step of:

selecting one of said output terminals of said first memory element having a maximum driving ability and connecting

said selected output terminal with said scan data input terminal of said second memory element.

16. The method of designing a semiconductor integrated circuit of Claim 15,

wherein said element connecting step further includes a step of discriminating whether or not there exist any unconnected output terminals among said output terminals of said first memory element, and in the case where unconnected output terminals exist, selecting one of said unconnected output terminals having a maximum driving ability.

17. A method of designing a semiconductor integrated circuit comprising:

an element connecting step of connecting one of plural output terminals of a first memory element with a scan data input terminal of a second memory element having a scan test function,

wherein said element connecting step includes a step of:

connecting one of said output terminals of said first memory element having a design margin larger than a predetermined value with said scan data input terminal of said second memory element, said design margin being obtained as a difference between one cycle time of a clock signal and propagation time required for a signal to travel from each of said output terminals of said first memory element to another memory element or an external output port.

18. A method of designing a semiconductor integrated circuit comprising:

an element connecting step of connecting one of plural output terminals of a first memory element with a scan data input terminal of a second memory element having a scan test function,

wherein said element connecting step includes steps of:

on the assumption that each of said output terminals of said first memory element is connected with said scan data input terminal of said second memory element, calculating a design margin of each of said output terminals of said first memory element as a difference between one cycle time of a clock signal and propagation time required for a signal to travel from each of said output terminals of said first memory element to another memory element or an external output port; and

connecting one of said output terminals of said first memory element having a design margin calculated in the previous step larger than a predetermined value with said scan data input terminal of said second memory element.

19. A method of designing a semiconductor integrated circuit comprising:

an element connecting step of connecting one of plural output terminals of a first memory element having a scan data input terminal with a scan data input terminal of a second memory element having a scan test function,

wherein said element connecting step includes a step of:

selecting one of said output terminals of said first memory element having maximum delay time of a signal received

at said scan data input terminal of said first memory element and connecting said selected output terminal with said scan data input terminal of said second memory element.

20. A method of designing a semiconductor integrated circuit comprising:

an element connecting step of connecting one of plural output terminals of a first memory element having a scan data input terminal with a scan data input terminal of a second memory element having a scan test function,

wherein said element connecting step includes a step of:

selecting one of said output terminals of said first element having delay time of a signal received at said scan data input terminal of said first memory element larger than a predetermined value and connecting said selected output terminal with said scan data input terminal of said second memory element.